Product Specification

Part Name: 9.0 inch TFT Display Module
Customer Part ID:
Topovision Part ID: TVT0900G2-H
Ver: B

Customer:
Approved by

From: Topovision Technology Co.,Ltd.
Approved by

Notes:

1. Please contact Topovision Technology Co., Ltd. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Topovision Technology Co., Ltd. for any intellectual property claims or other problems that may result from application based on the module described herein.

Contents

Revision History

Rev.	Date	Contents	Written	Approved
A	2015/08/26	Preliminary Specification	ZHENG	Ma
B	2017/07/26	Add two tapes to protect the FPC	ZHENG	Ma

Special Notes

Note1.	

1. OVERVIEW

TVT0900G2-H is 9” color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs ,control circuit and LED backlight. By applying 1024×600 images are displayed on the 9” diagonal screen. Display 16.2M colors by R.G.B signal input.

General specification are summarized in the following table:

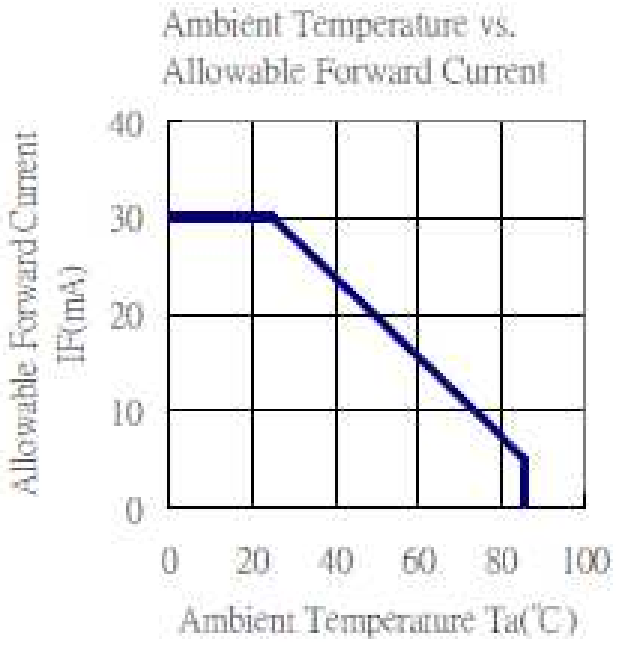
ITEM	SPECIFICATION			
Display Area (mm)	196.608(W) x 114.15(H)			
Number of Pixels	1024(H) × 3 (RGB) × 600(V)			
Pixel Pitch (mm)	0.192(W) x 0.19025(H)			
Color Pixel Arrangement	RGB vertical stripe			
Display Mode	Normally white			
Number of Colors	16.2M			
Brightness (cd/m^2)	500nit(typ)			
Response Time (ms)	25ms(typ.)			
Contrast Ratio	500(typ)			
Viewing Angle (CR≧10)	140degree (Horizontal.)			
	120degree (Vertical)			
Power Consumption (W)	2.736(typ.)			
Interface connection	LVDS			
Module Size (mm)		Min.	Typ.	Max.
	Horizontal (H)	210.9	211.1	211.3
	Vertical (V)	126.3	126.5	126.7
	Depth (D) w/o FPC	5.6	5.8	6.0
Module Weight (g)	TBD			
Backlight Unit	LED			
Surface Treatment	Anti-Glare, 3H			

2. ABSOLUTE MAXIMUM RATINGS

The following are maximun values which, if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VDD VDD_LVDS	-0.3	3.96	V	
Analog Supply Voltage	AVDD	-0.5	14.85	V	
Gate On Voltage	VGH	-0.3	40	V	
Gate Off Voltage	VGL	-20	0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	-0.3	40	V	
Signal Input Voltage	NIN0 ~ NIN3 PIN0 ~ PIN3 NINC,PINC	-0.5	5	V	
Forward Current (per LED)	If	-	30	mA	
Reverse Voltage (per LED)	VR	-	5	V	
Pulse forward current (per LED)	Ifp	-	35	mA	Note 1、2
Operation Temperature	T_{op}	-20	70	℃	Note 3
Storage Temperature	T_{stg}	-30	80	℃	Note 3

Note1：Ifp Conditions ： Duty≦1/10@ Pulse Width≦10msec
Note2：Each one of LED operation must be follow diagram of Ambient Temperature and Allowable Forward Current.



Note3：If users use the product out off the environmemtal operation range（temperature and humidity）, it will have visual quality concerns.

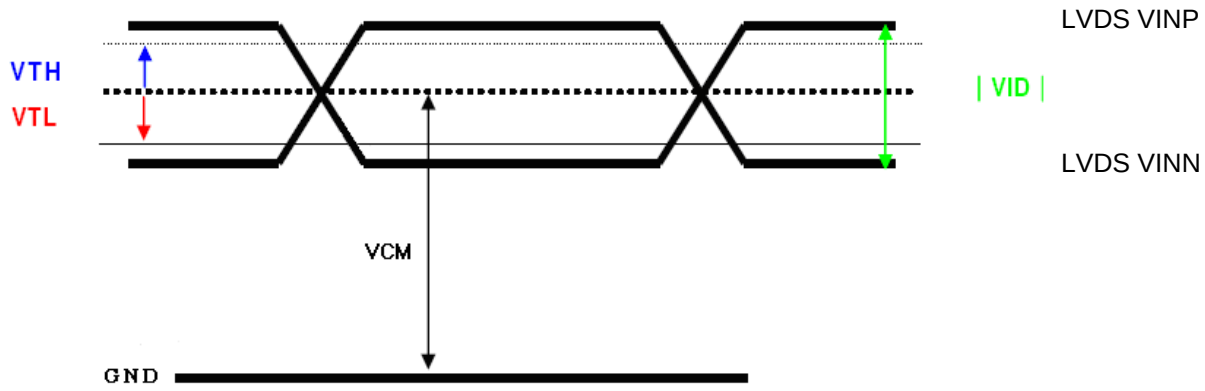
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	DVDD DVDD_LVDS	3	3.3	3.6	V	
Logic Input Voltage (LVDS:IN+,IN-)	VCM	$\frac{\lvert VID \rvert}{2}$	-	$2.4-\frac{\lvert VID \rvert}{2}$	V	Note1
	$\lvert VID \rvert$	200	-	600	mV	Note1
	VTH	-	-	100	mV	VCM=1.2V Note1
	VTL	-100	-	-	mV	
Analog Power Supply Voltage	AVDD	8.9	9.2	9.5	V	
Gate On Power Supply Voltage	VGH	17	18	19	V	
Gate Off Power Supply Voltage	VGL	-7	-6	-5	V	
Common Power Supply Voltage	VCOM	(3.21)	(3.41)	(3.61)	V	Note2

Note1：LVDS signal



Note2：Please adjust VCOM to make the flicker level be minimum.

3.2 TFT-LCD Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Gate on power current	IVGH	VGH =18V	-	0.5	1	mA	Note1
Gate off power current	IVGL	VGL= -6V	-	0.5	1	mA	Note1
Digital power current	IVDD	VDD = 3.3V	-	30	40	mA	Note1
Analog power current	IAVDD	AVDD = 9.2V	-	35	50	mA	Note1
Total Power Consumption	PC		-	447	636	mW	Note1

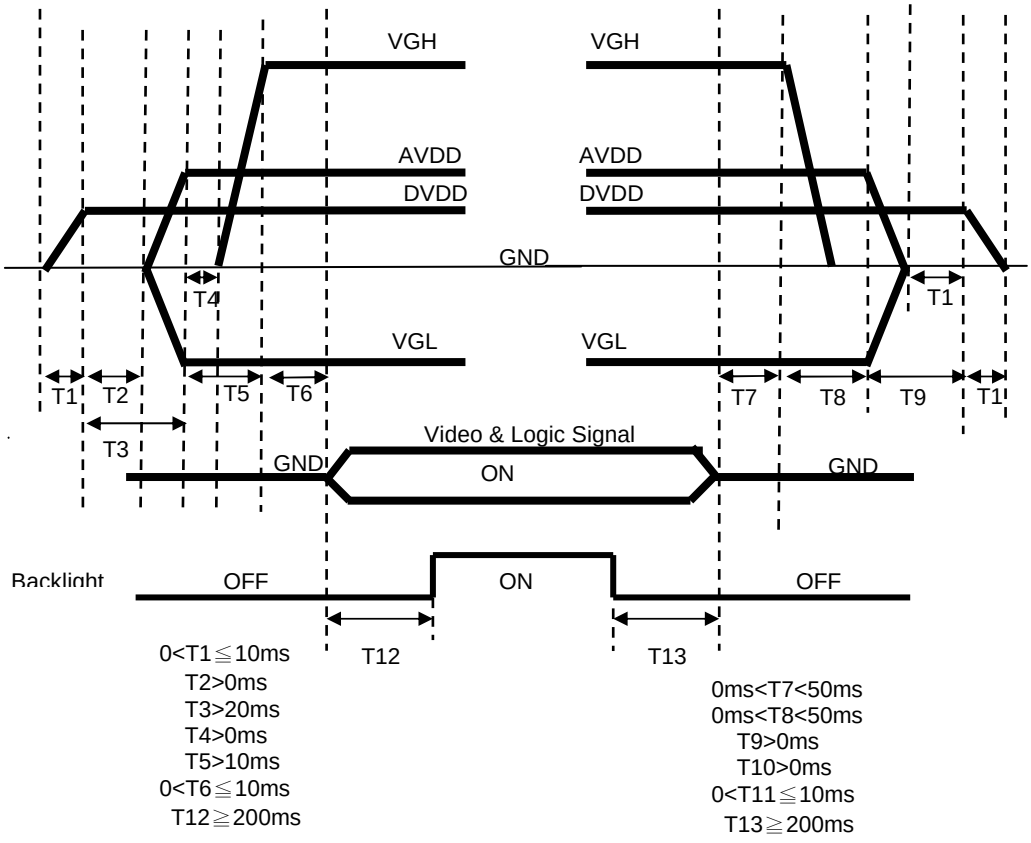
Note1：Typical: Under 256 gray pattern
Maximum: Under black pattern

256 gray pattern

Black Pattern

3.3 Power、Signal sequence

Power On：DVDD→AVDD/VGL→VGH→Video &Logic Signal→Backlight
Power Off：Backlight→Video &Logic Signal→VGH→AVDD/VGL→DVDD



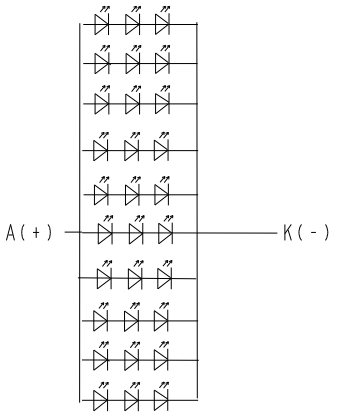
3.4 Backlight

Ta=25℃

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
LED current	IL	Ta=25℃ (20mA/serise)	--	200	–	mA	
LED voltage	VL	Ta=25℃ (20mA/serise)	8.4	9.3	10.5	V	
Power consumption	WL	Ta=25℃ (20mA/serise)	--	2.1	–	W	
LED Lifetime	-	Ta=25℃ IF=20mA	20000	--	--	Hr	

Remarks：

*1) LED Circuit Diagram



*2) A：Anode(＋)，K：Cathode(－)

*3) Suggestion: Using the constant current control to avoid the leakage light and brightness quality issue.

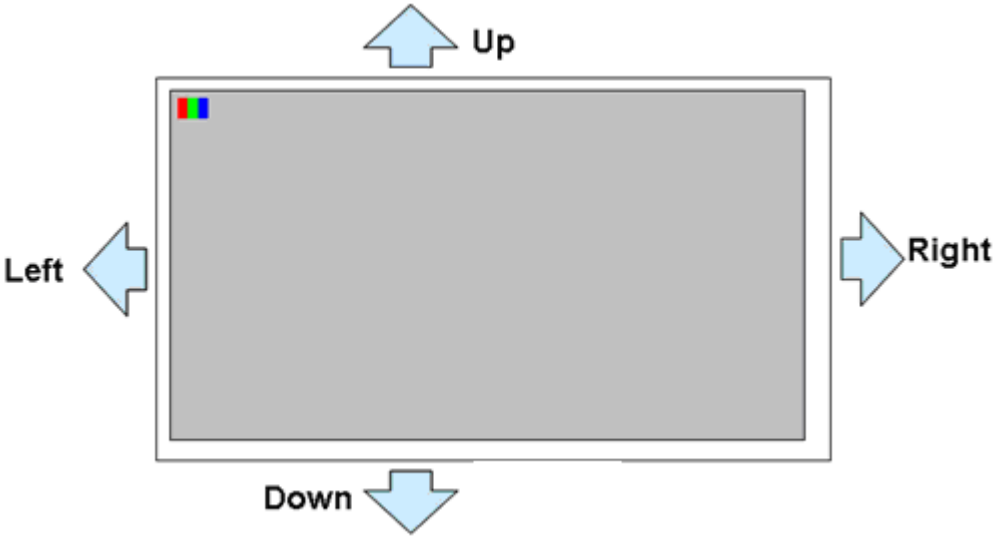
*4) Definition of Led lifetime：Luminance < Initial luminance 50%.

4. INTERFACE CONNECTION

4.1 CN1 (Input Signal)

PIN NO	SYMBOL	DESCRIPTION
1	VCOM	Common voltage
2	DVDD	Digital power
3	DVDD	Digital power
4	NC	Not connect
5	RESET	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10KΩ，C=1μF)
6	U/D	Vertical inversion
7	L/R	Horizontal inversion
8	STBYB	Standby mode, normally pull high STBYB=”1”, normal operation STBYB=”0”,timing control, source driver will turn off, all output are high-Z
9	GND	Ground
10	NINC	Negative LVDS differential clock inputs
11	PINC	Positive LVDS differential clock inputs
12	GND	Ground
13	NIND0	Negative LVDS differential data inputs
14	PIND0	Positive LVDS differential data inputs
15	GND	Ground
16	NIND1	Negative LVDS differential data inputs
17	PIND1	Positive LVDS differential data inputs
18	GND	Ground
19	NIND2	Negative LVDS differential data inputs
20	PIND2	Positive LVDS differential data inputs
21	GND	Ground
22	NIND3	Negative LVDS differential data inputs
23	PIND3	Positive LVDS differential data inputs
24	GND	Ground
25	SELB	6-bit/8-bit input select SELB = L , 8-bit ; SELB = H , 6-bit
26	GND	Ground
27	AVDD	Power for Analog Circuit
28	GND	Ground
29	VGH	Positive power for TFT
30	NC	Not connect
31	NC	Not connect
32	VGL	Negative power for TFT
33	GND	Ground
34	NC	Not connect
35	NC	Not connect
36	NC	Not connect
37	NC	Not connect
38	NC	Not connect
39	NC	Not connect
40	NC	Not connect

UD	LR	FUNCTION
0	1	Normal display
0	0	Inverse Left and Right
1	1	Inverse Up and Down
1	0	Inverse Left and Right Inverse Up and Down



4.2 CN2 (LED backlight)

PIN NO	SYMBOL	FUNCTION
1	A	Anode
2	K	Cathode

Note：
Maker:JST
Input connector : SHR-02V-S AWG#28 1.0A
Outlet connector: SSH-003T-P0.2-H

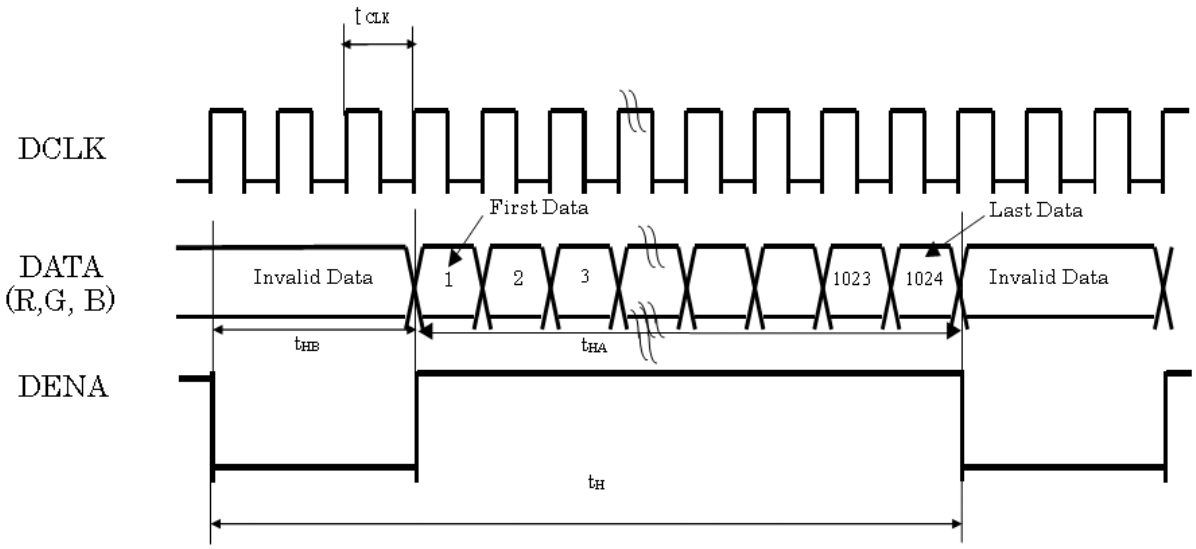
5. INPUT SIGNAL(DE ONLY MODE)

5.1 Timing Range

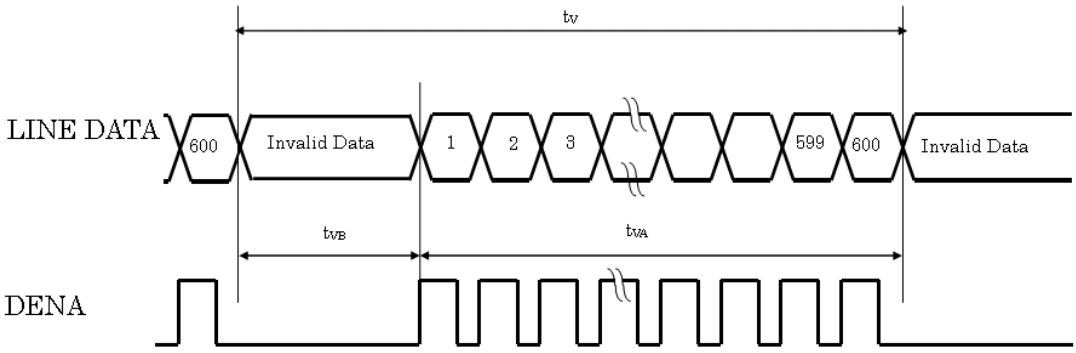
Category	Parameter	Unit	Min	Typ	Max
Timings	Frame Rate	Hz	55	60	65
Scanning Method	Gate Scanning Method (single / double)	Double			
Line Impedance	Capacitive Load of a Signal Line	pF	37.96	54.09	71.89
	Capacitive Load of a Gate Line	pF	178.78	190.99	207.43
	Resistance Load of Signal Line	KOhm	3.65	5.07	8.19
	Resistance Load of Gate Line	KOhm	2.87	3.32	3.95

5.2 Timing sequence(Timing chart)

5.2.1 Horizontal Timing Sequence

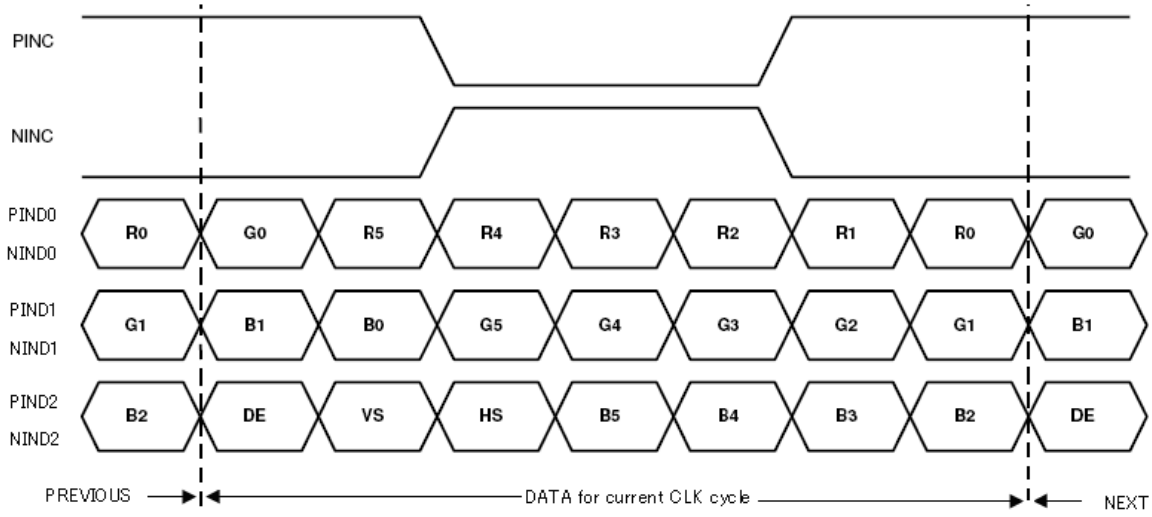


5.2.2 Vertical Timing Sequence

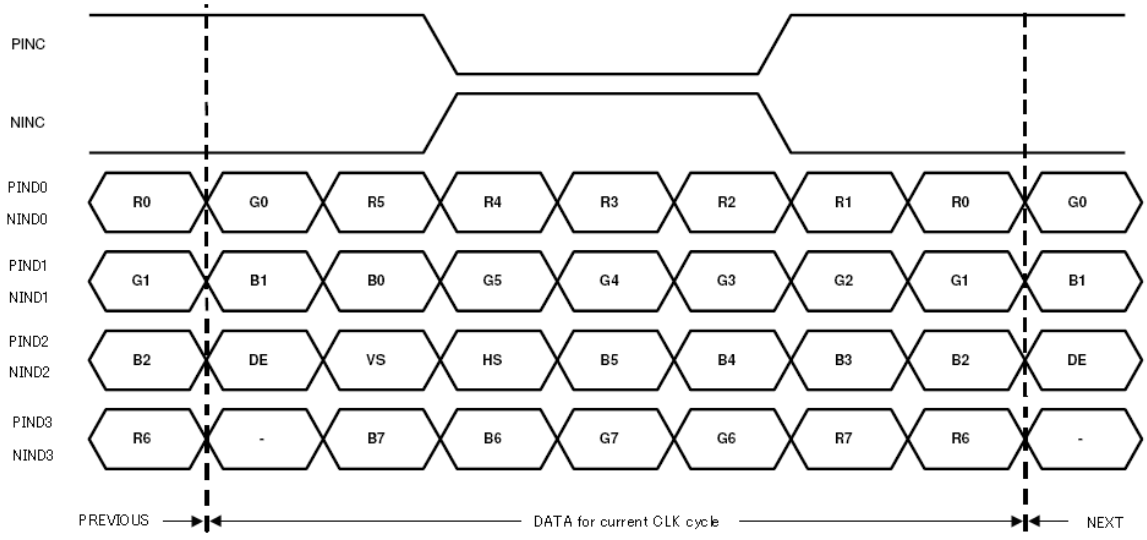


5.2.3 LVDS Input Data mapping

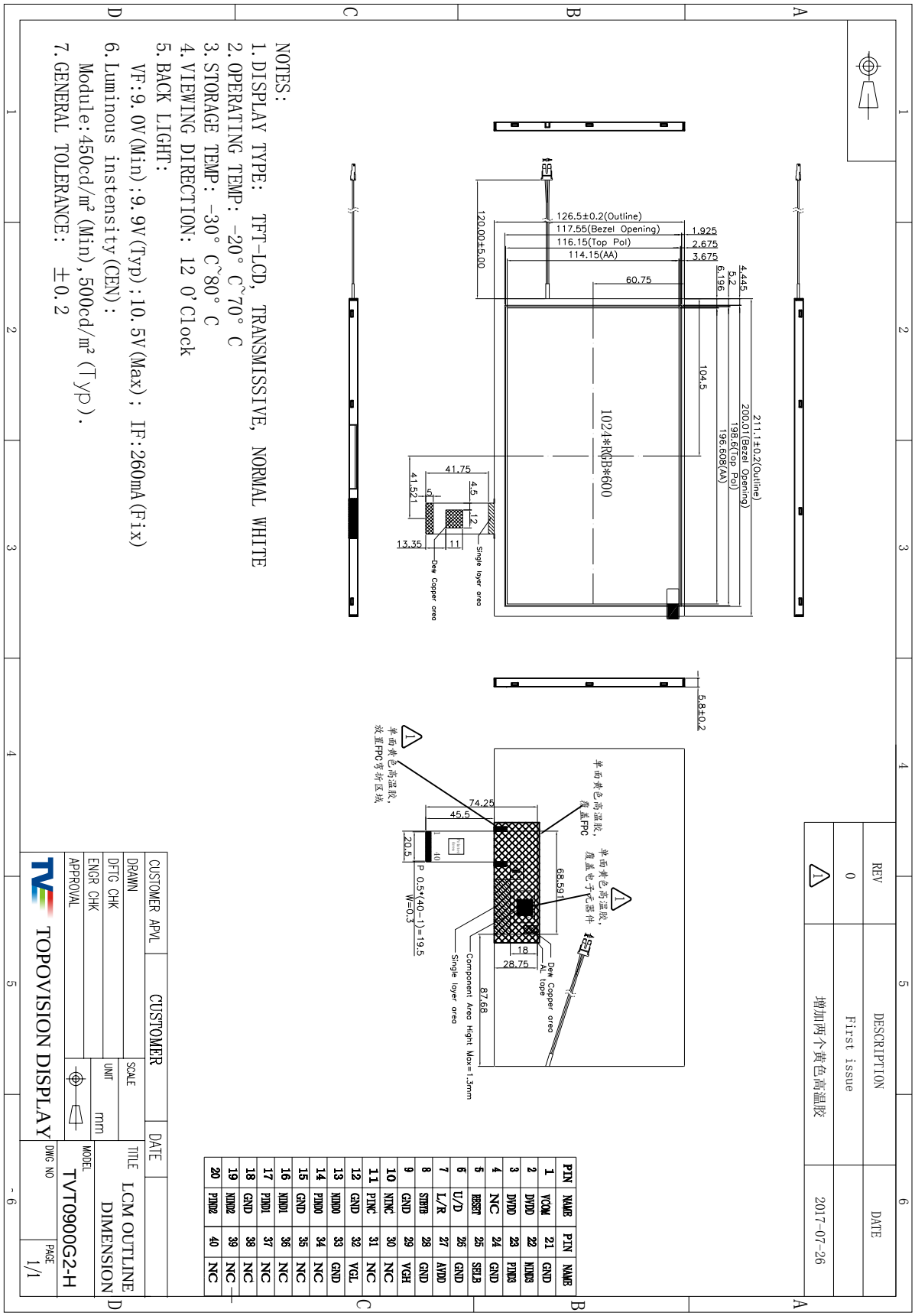
6 Bit LVDS input



8 Bit LVDS input



6. MECHANICAL DIMENSION

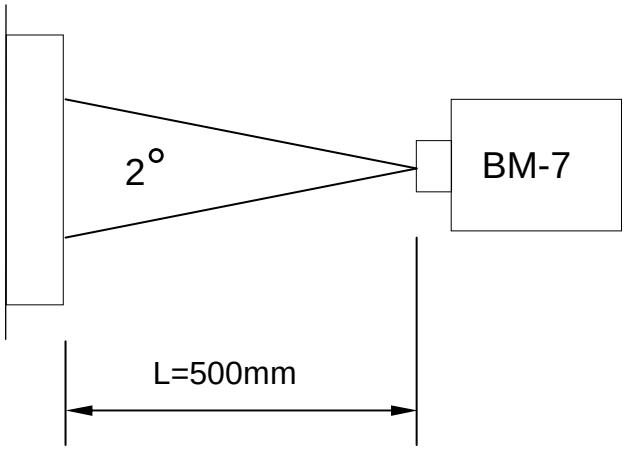


7. OPTICAL CHARACTERISTICS

Ta = 25℃, VCC=3.3V

ITEM		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Constrast Ratio		CR	Point-5	----	500		--	1, 2, 3
Luminance(CEN)		Lw	Point-5	450	500		cd/m^2	1, 3
Luminance Uniformity		ΔL		70	80		%	1, 3
Response Time (White - Black)		Tr +Tf	Point-5	-	25	40	ms	1, 3, 5
Viewing Angle	Horizontal	Left(ϕ)	CR≧10 Point-5	60	70	--	°	1, 3
		Right(ϕ)		60	70	--	°	
	Vertical	Upper(θ)		60	70	--	°	1, 2, 4
		Down(θ)		60	70	--	°	
Color Coordinate	White	Wx Wy	Point-5	TYP. -0.03	0.314 0.337	TYP. +0.03	--	1, 3

Note1： Measure condition: 25℃±2℃, 60±10%RH, under10 Lux in the dark room.BM-7 (TOP CON), viewing angle2°, IL=260 mA（Backlight current）, measurement after lighting on 10 mins.



Note2：Definition of contrast ratio：
Contrast Ratio (CR)= (White) Luminance of ON ÷ (Black) Luminance of OFF

Note3： Definition of luminance：Measure white luminance on the point 5 as figure.7-1
Definition of Luminance Uniformity: Measure white luminance on the point1~9 as figure.7-1
△L = [L(MIN)/L(MAX)]×100

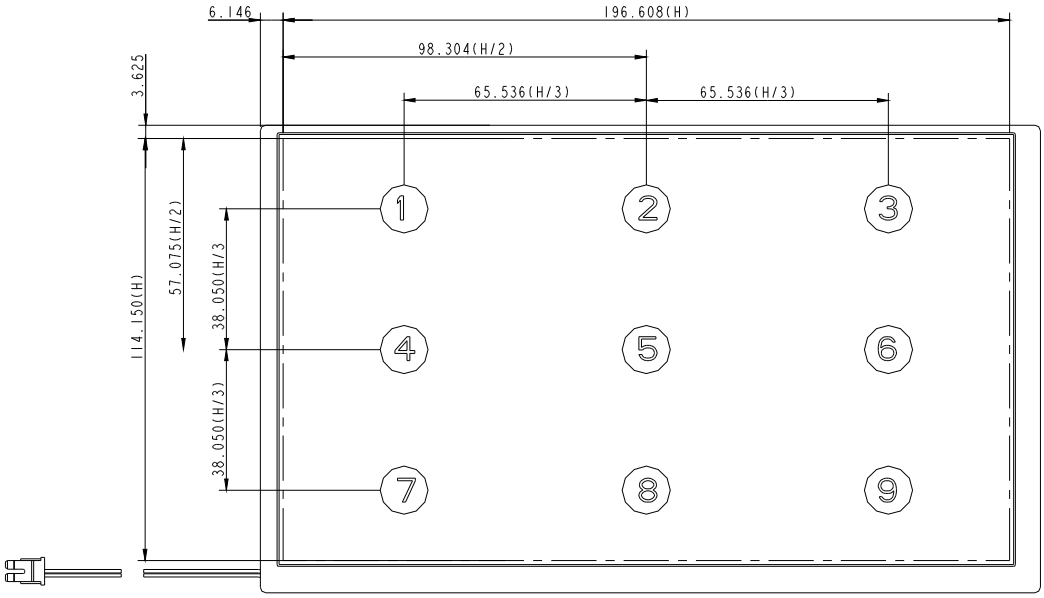


Fig.7-1 Measuring point

Note 4：Definition of Viewing Angle(θ,ψ),refer to Fig.7-2 as below：

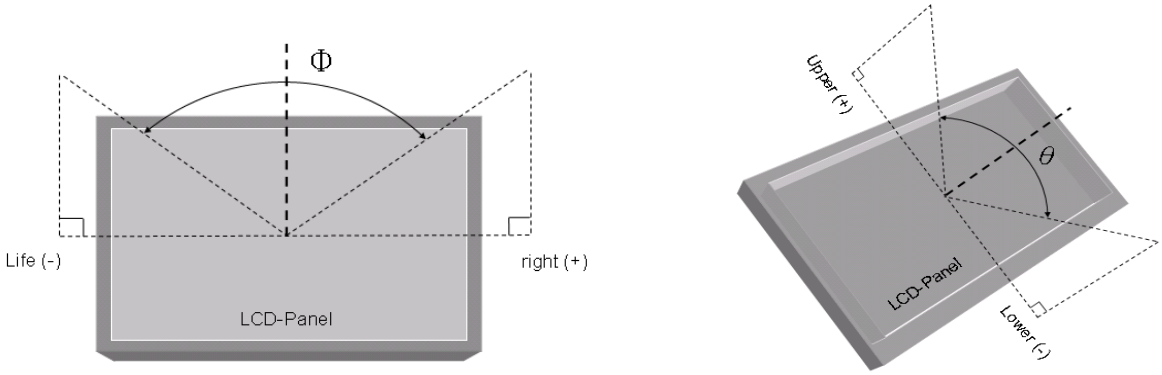


Fig.7-2 Definition of Viewing Angle

Note5：Definition of Response Time.(White-Black)

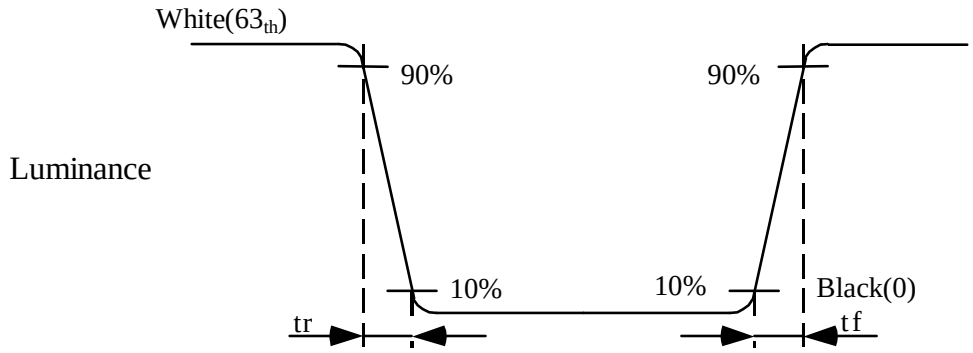


Fig.7-3 Definition of Response Time(White-Black)

8. RELIABILITY TEST

8.1 Temperature and humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	70℃ ;240hrs	
High Temperature Storage	80℃ ; 240hrs	
High Temperature High Humidity Operation	60℃ ; 90%RH ;240hrs	No condensation
Low Temperature Operation	-20℃ ; 240hrs	Backlight unit always turn on
Low Temperature Storage	-30℃ ; 240hrs	
Thermal Shock	–20℃(0.5hr) ~ 70℃(0.5hr) ; 100 Cycles	
Image Sticking	25℃ ; 4hrs	

Note 1：
Condition of Image Sticking test：25 ℃± 2 ℃
Operation with test pattern sustained for 4 hrs, then change to mid-gray pattern immediately.
After 5 mins, the mura must be disappeared completely .

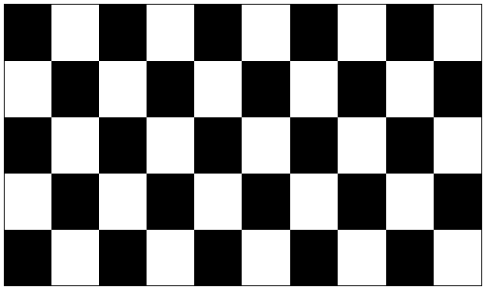


Image Sticking –pattern


Mid-Gray pattern

8.2 Shock and Vibration

TEST ITEMS	CONDITIONS
Shock (Non-operation)	● Shock level: 980m/s^2(equal to 100G). ● Waveform: half sinusoidal wave,6ms. ● Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of three shock inputs.
Vibration (Non-operation)	● Frequency range:8~33.3Hz ● Stoke：1.3 mm ● Vibration: sinusoidal wave, perpendicular axis(both x, y,z axis: 2Hrs). ● Sweep: 2.9G,33.3 Hz -400 Hz ● Cycle: 15 min

8.3 Electrostatic Discharge

TEST ITEM	CONDITIONS	Note
ESD	150pF，330Ω，±8kV&±15kV air& contact test	1
	200pF，0Ω，±200V contact test	2

Note： Measure
1: LCD glass and metal bezel
2: IF connector pins

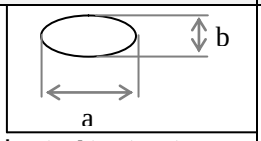
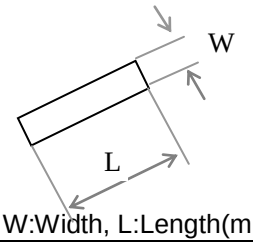
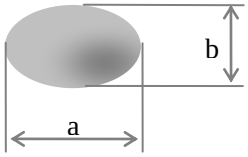
8.4. Judgment standard

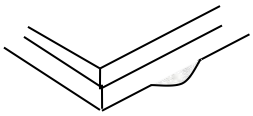
The Judgment of the above test should be made as follow:
Pass: Normal display image and no line defect.
Partial transformation of the module parts should be ignored.
Fail: No display image, Function NG, or line defects.

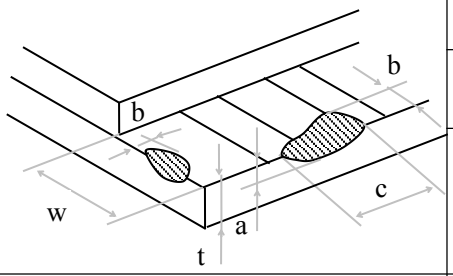
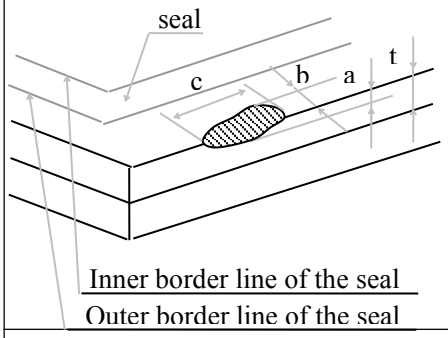
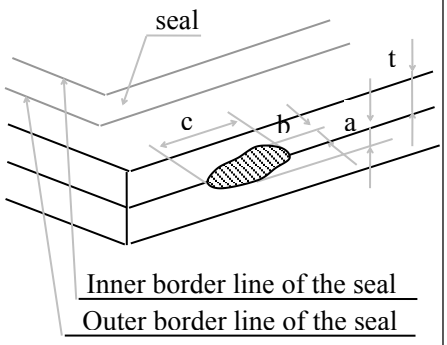
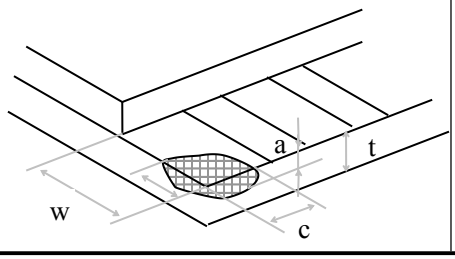
9. PACKING

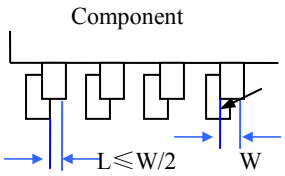
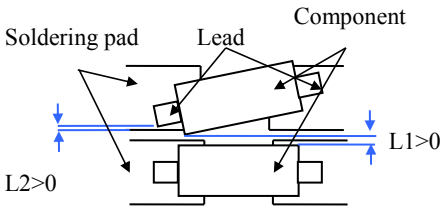
TBD.

10. INSPECTION CRITERION

<table>
<tr><th colspan="3" rowspan="3">Inspection item</th><th colspan="3">Judgement standard</th></tr>
<tr><th colspan="2" rowspan="2">Category</th><th>Acceptable number</th></tr>
<tr><th>A zone</th><th>B zone</th></tr>
<tr><td rowspan="6">1</td><td rowspan="2">Black spot, White spot, Bright Spot, Pinhole Foreign Particle, Bubble and Particle Between polarizer and glass, scratch on polarizer</td><td rowspan="2"> 
Φ =(a+b)/2(mm)</td><td>A
B
C
D</td><td>Φ≦0.15
0.15<Φ≦0.20
0.20<Φ≦0.30
0.30<Φ</td><td>Ignored
2
1
0</td><td rowspan="2">Ignored</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td><td>3</td></tr>
<tr><td rowspan="4">Pixel point defect</td><td>Bright spot</td><td colspan="2">0.15<Φ≦0.20</td><td>N≤0</td><td rowspan="4">Ignored</td></tr>
<tr><td>Dark spot/ Black spot</td><td colspan="2">0.15<Φ≦0.20</td><td>N≤2</td></tr>
<tr><td>Attached to the two pixels are bright spots</td><td colspan="2">0.15<Φ≦0.20</td><td>N≤0</td></tr>
<tr><td>Even a two pixel is dark</td><td colspan="2">0.15<Φ≦0.20</td><td>N≤0</td></tr>
<tr><td>Pixel total number</td><td colspan="2">0.15<Φ≦0.20</td><td>N≤2</td><td></td></tr>
<tr><td colspan="5">Note1: the spot defect caused by foreign matter is judged according to the defect of the foreign body.
Note 2: when the light is not wired to show the type of defects.</td><td></td></tr>
<tr><td>2</td><td>Black line, White line, Bubble and Particle Between Polarizer and glass, Scratch on polarizer</td><td> 
W:Width, L:Length(mm)</td><td>A
B
C
D</td><td>W≦0.01
0.01<W≦0.03 L≦3.0
0.03<W≦0.05 L≦3.0
0.05<W</td><td>Ignored
2
1
0</td><td>Ignored</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td><td>2</td></tr>
<tr><td>3</td><td>Contrast variation</td><td> 
Φ=(a+b)/2(mm)</td><td>A
B
C
D</td><td>Φ≦0.2
0.2<Φ≦0.3
0.3<Φ≦0.4
0.4<Φ</td><td>Ignored
2
1
0</td><td>Ignored</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td><td>3</td><td></td></tr>
<tr><td>4</td><td>Bubble inside cell</td><td></td><td colspan="2">any size</td><td>none</td><td>none</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">Polarizer defect (if Polarizer is used)</td><td>Scratch and damage on polarizer, particle on polarizer or between polarizer and glass.</td><td colspan="4">Refer to item 1 and item 2.</td></tr>
<tr><td>Bubble, dent and convex</td><td>A
B
C</td><td>Φ≦0.2
0.2<Φ≦0.3 distance >5
0.3<Φ</td><td>Ignored
5
0</td><td>Ignored</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td><td>3</td><td></td></tr>
</table>

Inspection item		Judgement standard		
		Category	Acceptable number	
			A zone	B zone
6	Surplus glass	①Stage surplus glass 	b≦0.3mm	
		②Surrounding surplus glass 	Should not influence outline dimension and assembling.	
7	MURA	①MURA	Naked eye examination: red, green, blue screen does not allow the appearance, black screen requires visual is not obvious, the specific reference limit samples. Note: the principle of closing the sample is to be installed on the whole machine and the end user will not find it in the normal usage scenario. Inspection basis: 6%ND (MURA mainly in the black screen and indoor light is relatively dark will be found, it is recommended to turn off the indoor lighting inspection.)	
		②Point Black / White / point(MURA)	1, under the black / gray screen check: D≦0.10mm Ignored; 0.10mm<D≦0.3mm, N≦2; D>0.3mm: Unqualified。 2, switch to the red, green, blue in which any one of the screen appears black or white or point to point white or point of failure. 	

<table>
<tr><th colspan="3" rowspan="2">Inspection item</th><th colspan="2">Judgment standard</th></tr>
<tr><th colspan="2">Category(application: B zone)</th></tr>
<tr><td rowspan="5">8</td><td rowspan="5">Glass defect crack</td><td rowspan="4">①The front of lead terminals
 
</td><td>A</td><td>If a≦t and b ≦1.0, c is not limited</td></tr>
<tr><td>B</td><td>a≦t, 1≦b≦2mm, c≦3mm</td></tr>
<tr><td>C</td><td>If glass crack cover alignment mark, b≦0.5mm.</td></tr>
<tr><td>D</td><td>Crack at two sids of lead terminals should not cover patterns and alignment mark</td></tr>
<tr><td>②Surrounding crack—non-contact side
 
</td><td colspan="2">b < Inner borderline of the seal</td></tr>
<tr><td>③ Surrounding crack— contact side
 
</td><td colspan="2">b < Outer borderline of the seal</td></tr>
<tr><td>④Corner
 
</td><td>A</td><td>a ≦ t, b ≦ 3.0, c ≦ 3.0
*Glass crack should not cover patterns used for</td></tr>
</table>

Inspection item			Judgement standard
9	FPC defect	Component soldering: No cold soldering, short/open circuit, burr, tin ball. The flat encapsulation component position deviation must be less than 1/2 width of the pin (Pic.1)； The sheet component deviation: pin deviates from the pad and contact with the near components is not permitted（Pic.2）	
		lead defect: The lead lack must be less than 1/2of its width; The lead burr must be less than 1/2 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted